24. (New) The shift register as set forth in claim 20, wherein the level shifters operate in response to the input pulse that has been successively transmitted.

25. (New) The shift register as set forth in claim 24, further comprising:

a judging section, which identifies, based on the input pulse and an output signal, a level shifter which corresponds to blocks requiring no clock signal input, so as to control the input pulse into the level shifter.

REMARKS

Applicants appreciate the Examiner's thorough examination of the subject application and, further, request reconsideration of the subject application based on the foregoing amendment and the following remarks.

Claims 1-25 are pending in the subject application. Claims 1 and 20 have been amended, and new claims 22-25 have been added by the present amendment. The amendments are fully supported by the specification as originally filed.

Applicants claim a shift register including: a plurality of flip flops that output a signal in synchronization with a clock signal, and a plurality of level shifters for level-shifting the clock signal, wherein each level shifter is provided for a predetermined number of flip flops. As recited in claim 1, the flip flops are divided into a plurality of blocks each including at least one flip flop, and a level shifter is provided for each of the blocks.

The Applicant's invention is exemplified by shift register 11, as shown in FIG. 1. The shift register 11 can be used as a shift register for at least one of the data signal line driving circuit and the scanning signal line driving circuit (see FIG. 2). The shift register 11 includes set/reset flip flops $F1_{(i)}$..., a flip flop section 12 operating at the driving voltage V_{cc}, and level shifters $13_{(i)}$... which increase the voltage of a clock signal CK to

the flip flops $F1_{(1)}$... The level shifters are capable of increasing the voltage to the flip flops even when an amplitude of the clock signal CK is smaller than the driving voltage V_{cc} (see specification at page 16, last two paragraphs).

With reference to claim 1, when the flip flop $F1_{(i)}$ does not require input of a clock signal $CK_{(i)}$, operation of the level shifter $13_{(i)}$ is suspended. In such a state, the clock signal $CK_{(i)}$ is not driven, so that there is no power consumption required for driving. Therefore, although the shift register can include a large number (n) of current-driving level shifters, power is consumed only by the level shifter in operation.

Claims 1-21 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 6,232,945 to Moriyama et al. (hereinafter "Moriyama") in view of U.S. Patent 6,081,131 to Ishii. This rejection is respectfully traversed.

Moriyama is directed to a common display device and a shift register used therefor, but fails to teach or suggest a level shifter. In Moriyama, embodiments (1) through (6) use a decoder for the video signal line driving circuit 291 and the scanning line driving circuit 293 (see column 14, lines 43-46). In a seventh embodiment, Moriyama teaches a shift register circuit 21 "composed of 853-units of D type flip-flops 22_1, ..., 22_{853} corresponding to the number of the horizontal pixels" (see column 14, line 65 to column 15, line 6). In Moriyama, the flip-flops are connected in series, and each flip-flop transfers a start pulse to the succeeding flip-flop in synchronism with a clock pulse (see column 15, lines 11-19). However, Moriyama fails to teach or suggest use of a level shifter.

Ishii fails to remedy the deficiencies of Moriyama. Ishii relates to a logical amplitude level conversion circuit in a liquid crystal device. As shown in FIG. 8, Ishii teaches level shifters 51-54 which are provided outside a driver 48. Therefore, Ishii fails to teach or suggest a plurality of level shifters wherein a level shifter is provided for each of a predetermined number of flip flops, as required in the independent claims.

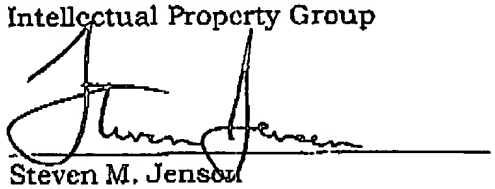
The combined teachings of Moriyama in view of Ishii fail to teach or suggest the Applicants' claimed invention, e.g., as recited in claims 1 and 20. In Ishii, the level shifters 51-54 are provided outside the driver 48. There is no teaching or suggestion in Ishii for providing a level shifter that is connected to a corresponding predetermined number of flip flops, and thus one of ordinary skill in the art would not be capable of combining Moriyama and Ishii in such a manner.

Moreover, with reference to claim 1, there is no teaching in Moriyama and/or Ishii for suspending operation of a level shifter when a corresponding flip flop does not require input of a clock signal.

For the above reasons, the claims should now be in condition for immediate allowance. However, if there are any outstanding issues, the Examiner is urged to call the undersigned at the phone number listed below.

The Applicants believe that additional fees are not required for consideration of the within Amendment. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. 04-1105.

Respectfully submitted,
EDWARDS & ANGELL, LLP
Dike Bronstein Roberts & Cushman
Intellectual Property Group

Date: August 7, 2002 By: 

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APPENDIX A:
VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claims 1 and 20 have been amended as follows:

1. (Amended) A shift register, comprising:

flip flops of a plurality of steps that [operate] output a signal in synchronization with a clock signal, and

a level shifter for increasing a voltage of a clock signal smaller in an amplitude than a driving voltage of said flip flop and for applying the clock signal to each of said flip flops, said shift register transmitting an input pulse in synchronization with the clock signal,

wherein said flip flops are divided into a plurality of blocks, each including at least one of said flip flops,

said level shifter is provided for each of said blocks, and

among a plurality of said level shifters, at least one of said level shifters, which correspond to blocks requiring no clock signal input for transmitting the input pulse, is suspended at that point.

20. (Amended) A shift register, in which a plurality of flip flops are connected, for transmitting an input pulse in synchronization with a clock signal and for outputting a signal,

said shift register comprising a plurality of level shifters for level-shifting [a] the clock signal, said level shifter being provided for every predetermined number of said flip flops.

The following new claims have been added:

22. (New) The shift register as set forth in claim 1, wherein the level shifter operates in response to the input pulse that has been successively transmitted.

23. (New) The shift register as set forth in claim 22, further comprising:

a judging section, which identifies, based on the input pulse and an output signal, a level shifter which corresponds to blocks requiring no clock signal input, so as to control the input pulse into the level shifter.

24. (New) The shift register as set forth in claim 20, wherein the level shifters operate in response to the input pulse that has been successively transmitted.

25. (New) The shift register as set forth in claim 24, further comprising:

a judging section, which identifies, based on the input pulse and an output signal, a level shifter which corresponds to blocks requiring no clock signal input, so as to control the input pulse into the level shifter.